

AMENDMENTS TO THE CLAIMS

1. (Currently amended) A method for processing signal values ~~in a digital signal processor, comprising the steps of:~~
in response to a single trellis instruction that specifies trellis state metrics for a time t_0 , based on the signal values, and transition metrics from time t_0 to time t_1 , for selected trellis states, a programmable digital signal processor executing the steps of:
adding a transition metric to a first state metric for time t_0 to provide a first value;
subtracting the transition metric from a second state metric for time t_0 to provide a second value;
for each selected trellis state, comparing the first and second values; and
selecting the maximum of the first and second values for each selected trellis state to provide trellis state metrics for time t_1 , wherein the adding, subtracting, comparing and selecting operations ~~of the single trellis instruction~~ are executed by the digital signal processor ~~in a single clock cycle of the digital signal processor and wherein the first value, the second value, a result of the comparison and the trellis state metrics for time t_1 are determined in the single clock cycle of the digital signal processor~~ response to the single trellis instruction.
2. (Previously presented) A method as defined in claim 1, further comprising the step of, for each selected trellis state, adding to the maximum value a correction factor that is a function of the first and second values.
3. (Original) A method as defined in claim 2, wherein the step of adding a correction factor comprises accessing a lookup table containing correction factors.
4. (Original) A method as defined in claim 1, wherein the trellis instruction implements a forward trellis function for calculating α trellis state metrics.

5. (Original) A method as defined in claim 1, wherein the trellis instruction implements a reverse trellis function for calculating β trellis state metrics.

6. (Original) A method as defined in claim 1, wherein the trellis instruction simultaneously implements a forward trellis function for calculating α trellis state metrics and a reverse trellis function for calculating β trellis state metrics, using a single instruction, multiple data approach.

7.-17. (Canceled)

18. (Currently amended) A processor for processing signal values, comprising:
a memory for storing instructions and operands for digital signal computations;
a program sequencer for generating instruction addresses for fetching selected ones of said instructions from said memory; and

a computation block comprising a register file for temporary storage of operands and results and an accelerator for executing a trellis instruction that specifies trellis state metrics for a time t_0 and transition metrics from time t_0 to time t_1 , wherein the trellis state metrics are based on the signal values, said accelerator comprising an adder for adding a transition metric to a first state metric for time t_0 to provide a first value, an adder for subtracting the transition metric from a second state metric for time t_0 to provide a second value, a comparator for determining the maximum of the first and second values for each trellis state and a data selector for selecting the maximum of the first and second values for selected trellis states to provide trellis state metrics for time t_1 , wherein the adders, the comparator and the data selector of the accelerator are configured to execute the adding, subtracting, comparing and selecting operations of the trellis instruction in a single clock cycle of the processor and wherein the first value, the second value, the maximum of the first and second values and the trellis state metrics for time t_1 are determined in the single clock cycle of the signal processor in response to a single trellis instruction.

19.-24. (Canceled)

25. (Previously presented) A processor as defined in claim 18, wherein the accelerator includes an additional adder to add to the maximum of the first and second values a correction factor that is a function of the first and second values.

26. (Previously presented) A processor as defined in claim 25, wherein the accelerator further comprises a lookup table containing correction factors.